semiconductor substrate is prepared in which a lightly doped layer 2 of a first conductive type is epitaxially grown on a heavily doped substrate 1 of the first conductive type to be a drain region. Then, a diffusion region 3 of a second conductive type referred to as a body region is formed from a surface of the semiconductor substrate by impurity implantation and high temperature thermal treatment at 1000°C or higher. Further, from the surface, a heavily doped impurity region 7 of the first conductive type to be a source region and a heavily doped body contact region 8 of the second conductive type for the purpose of fixing a potential of the body region by an ohmic contact are formed and are connected to a source electrode 7a and a body electrode 8a, respectively. Here, since a potential of the body contact region of the second conductive type and the potential of the body contact region of the second conductive type are the same, they are laid out so as to be in contact with each other in Fig. 1. The source electrode 7a and the body electrode 8a are connected with each other through a contact hole, not shown in the figure, for electrically contacting the two regions. These are structured in the same way as those of the conventional transistor. Then, a trench 4 is formed by etching single crystalline silicon through the source region of the first conductive type. A gate insulating film 5 is

formed in a U-shaped form on an inner wall of the silicon trench such that the gate insulating film 5 covers a side wall and a bottom surface of the trench and has an internal U-shaped void therein. Polycrystalline silicon 6 containing a high concentration of impurity is filled in a U-shaped form inside the internal void of the gate insulating film in the trench so that the polycrystalline silicon 6 itself has an internal U-shaped void with a sidewall and a bottom surface. Further, metal silicide 9 is formed inside the internal void of the polycrystalline silicon 6 film in the trench so as to be in contact with the polycrystalline silicon 6 along the direction of the trench. The polycrystalline silicon 6 containing a high concentration of impurity and the metal silicide 9 are connected to a gate electrode 9a. The heavily doped region of the first conductive type on a rear side of the semiconductor substrate is connected to a drain electrode 1a.--

IN THE CLAIMS:

Kindly amend claims 1 and 10 by rewriting them in amended form as follows:

1. (Three Times Amended) A vertical MOS transistor comprising: